International Journal of Engineering Science and Advanced Technology (IJESAT)

Vol 26 Issue 03(March),2026

Received: 19-02-2026 Accepted: 23-03-2026 Published: 31-03-2026

Performance Analysis of Squaring Circuits Across Different FPGA Architectures

Syed Saleem,
Dept. of Electronics and Communciation Engineering,
Annamacharya Institute of Technology and Sciences, Kadapa, India.
saleema7253362@gmail.com

Korrapadu Mahammad Haneef,
Dept. of Electronics and Communciation Engineering,
Annamacharya Institute of Technology and Sciences, Kadapa, India.
mahammad.hnf@gmail.com

Busireddy Pallavi
Dept. of Electronics and Communciation Engineering,
Annamacharya Institute of Technology and Sciences, Kadapa, India.
busireddypallavi5@gmail.com

Changa Thanuja,
Dept. of Electronics and Communciation Engineering,
Annamcharya Institute of Technology and Sciences, Kadapa, India.
thanujachanga409@gmail.com

Gattugari sai Sruthi,
Dept. of Electronics and Communciation Engineering,
Annamacharya Institute of Technology and Sciences, Kadapa, India.
sruthi84799@gmail.com

Boya Harsha Vardhan,
Dept. of Electronics and Communciation Engineering,
Annamacharya Institute of Technology and Sciences, Kadapa, India.
harh07346@gmail.com

Abstract*—Squaring Circuits are crucial for high speed and computational efficiency in embedded system, digital signal processing, and cryptography applications. Due to redundant operations, array multipliers used in Existing system increase power and time. By utilizing the symmetry of squaring Architecture that lowers Complexity, delay, and power. Implemented on Xlinix spartan-7, Artix-7, Kintex-7 FPGA, the 4-bit, 8-bit, and 16-bit circuits demonstrate enhanced latency and power efficiency. The design is scalable and appropriate for low power, high speed applications.

Keywords*—Squaring circuit, VLSI Design, FPGA Implementation, Low Power, Delay Optimization, hardware Efficiency, digital signal processing (DSP), Scalable Architecture.

I. INTRODUCTION

In modern VLSI system Arithmetic operations like multiplication and squaring are essential to applications like digital signal processing, cryptography, and embedded systems in contemporary VLSI systems. Efficient computing approaches have been developed in response to the increasing demand for low-power and high-speed architectures Because they can minimize hardware complexity, reduce power consumption, and enhance computational speed, Vedic mathematics-based designs have attracted a lot of attention [1], [3]. According to recent research, Vedic multipliers and squaring circuits outperform traditional methods, especially when used on FPGA systems [4], [5]. Scalability and performance in nanoscale architectures are further improved by the use of cutting-edge technology like FinFET [2]. Furthermore, optimization strategies including energy-efficient structures, hybrid compressors, and approximation computation approaches help to optimize the system as a whole [6], [8], and [11]. Furthermore, Vedic arithmetic has shown promise in real-world applications, particularly in cryptography and digital signal processing [7], [12]. Yavadunam and other Vedic sutra-based methods allow for simpler and speedier computing [10]. As a result, Vedic-based arithmetic circuits are becoming more widely acknowledged as a viable method for creating VLSI systems that are both high-performance and energy-efficient [9], [15].

II. LITERATURE SURVEY

1. Karthik Naregal, et al., (2017) -- Design and implementation of high efficiency Vedic binary multiplier circuit based on squaring circuits.

The paper presents a dedicated multiplier circuit using Nikhilam Sutra for efficient multiplication and squaring of binary numbers. It demonstrates significant area reduction by 69.8% and speed improvement by 28.2%, verified through implementation in Verilog HDL and synthesis using Xilinx ISE.

2. R. Sushma, et al., (2013) -- Area and Speed Efficient Arithmetic Logic Unit Design Using Ancient Vedic Mathematics on FPGA.

The paper highlights that Vedic mathematics, specifically the Urdhva and high-speed multipliers, achieving approximately 2 times faster performance and a 3% area reduction compared to traditional ALU architectures.

3. Sithara Raveendran, et al., (2018) -- FPGA Implementation of Square and Cube Architecture Using Vedic Mathematics.

The paper proposes new squaring architectures based on Vedic mathematics sutras, specifically Antyayordashakepi and Dwandwa Yoga, implemented on FPGA for 8 and 16-bit sizes, demonstrating efficient power delay products of 106.99 and 45.65 for the respective bit sizes.

4. K Sethi, et al., (2015) -- Multiplier less high-speed squaring circuit for binary numbers.

The paper traces how squaring circuits have evolved from traditional multiplier- based designs (using Booth's algorithm, Vedic multipliers) to more optimized multiplier-less architectures. Shows progression toward reducing hardware complexity and computation time.

5. Richa Sharma, et al., (2015) -- Design and FPGA implementation of optimized 32-bit Vedic multiplier and square architectures

ISSN 2250-3676 ijesat@gmail.com https://www.ijesat.com/

International Journal of Engineering Science and Advanced Technology (IJESAT)
Vol 26 Issue 03(March),2026
Received: 19-02-2026 Accepted: 23-03-2026 Published: 31-03-2026

The paper discusses the design of high-speed Vedic multiplier and squaring architectures, utilizing concatenation operations and a single carry save adder, resulting in significant speed improvements compared to existing designs, implemented on Xilinx Spartan-3E FPGA.

6. Deepa, et al., (2020) -- VLSI Design of a Squaring Architecture based on Yavadunam Sutra of Vedic Mathematics

The paper presents a VLSI design for squaring architecture utilizing the Yavadunam algorithm from Vedic Mathematics, addressing the need for efficient hardware implementation of squaring binary numbers, which is crucial for high-speed digital applications.

II. EXISTING SYSTEM

A squaring circuit is a specialized hardware device that uses operand symmetry to compute A × A. This method improves area, power consumption, and processing speed by eliminating redundant hardware processes, in contrast to traditional multipliers. These circuits are frequently used in digital signal processing and communication systems for tasks including power estimates, FFT, and RMS computation. Techniques like carry-save addition and Vedic mathematics are frequently used in their design to increase efficiency [14].

A. Existing n-Bit Squaring Circuit

The architecture uses parallel processing and improved addition algorithms to increase speed and power efficiency. The input is divided into two equal portions, their squares are processed independently, and the cross-product is calculated using a multiplier. The output is subsequently produced by final addition stages once the intermediate results are effectively merged using a carry save adder [17].

.

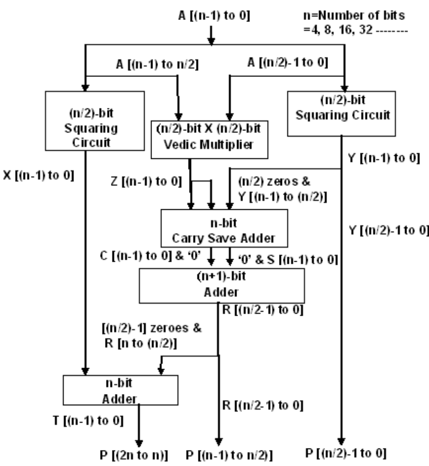

Fig. 1. Block Diagram of Existing Vedic-Based Squaring Circuit Architecture [17]

III. PROPOSED 4-BIT SQUARING CIRCUIT

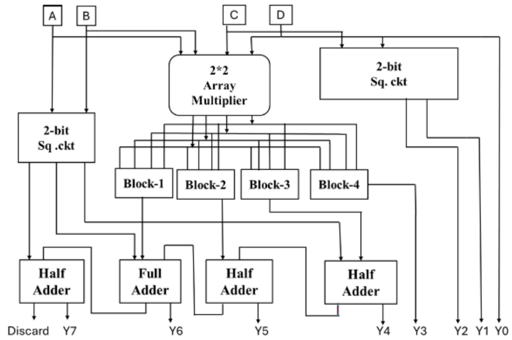

Fig. 2. Block Diagram of the Proposed 4-bit Squaring Circuit Architecture

N complete adders are connected in series to create an N-bit adder. Each stage adds matching bits and transfers the carry to the next, creating an additional carry-out bit. In a 4-bit squaring circuit, an array multiplier creates cross-products while the input is divided into two 2-bit portions and squared using 2-bit squaring blocks. An (N+1)-bit adder is used to combine the sum and carry outputs that the carry-save adder first generates. The carries are then propagated using an N-bit adder to produce the appropriate square result.

IV. RESULTS AND DISCUSSION

By improving the architecture and removing unnecessary processes, the suggested squaring circuits achieve lower delay and lower power consumption as compared to traditional designs. Among the FPGA families, Artix-7 offers a balanced trade-off between power and performance, Spartan-7 guarantees greater power efficiency, while Kintex-7 offers faster speed. Scalable from 4-bit to 16-bit, the design improves hardware utilization, performance, and energy economy.

In Fig.3. simulated waveform demonstrates that the output accurately generates the corresponding square values from 1 to 225, while the 4-bit input changes from 1 to 15. Correct partial product production and carry handling are confirmed by the output bits changing smoothly and without interruption. This confirms that the suggested 4-bit squaring circuit functions properly for any combination of inputs.

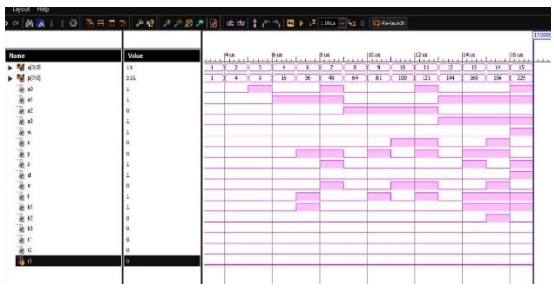

Fig. 3. Output Response of Proposed 4-Bit Squaring circuit

TABLE 1. Comparison of Proposed 4-Bit Squaring Circuit with Existing Literature

Reference	On-Chip Power(W)	Net Delay(nsec)	Gate Delay(nsec)	Total Dealy(nsec)
[18]	2.30	1.80	3.40	5.20

International Journal of Engineering Science and Advanced Technology (IJESAT)
Vol 26 Issue 03(March),2026
Received: 19-02-2026 Accepted: 23-03-2026 Published: 31-03-2026

[19]	2.25	1.70	3.30	5.00
Proposed (Kintex-7)	2.202	1.252	2.959	4.211
Proposed (Spartan-7)	2.105	1.630	3.191	4.822
Proposed (Artix-7)	2.145	1.419	2.979	4.398

When compared to traditional designs and current techniques in the literature, the suggested 4-bit squaring circuit performs better in terms of decreased latency and increased power efficiency. While the methods in [10]- [13] mostly focus on architectural improvements, the suggested design optimizes power and delay more successfully, which makes it ideal for high-speed and energy-efficient VLSI applications.

V. Conclusion

The suggested squaring circuit architecture shows notable gains in hardware efficiency, power consumption, and latency compared to traditional and current approaches. The approach achieves improved performance appropriate for high-speed VLSI applications by efficiently utilizing the symmetry present in squaring operations and removing unnecessary computations. FPGA implementation across many families reveals that Artix-7 offers a well-balanced compromise between performance and energy consumption, Spartan-7 is more power-efficient, while Kintex-7 gives the fastest speed. The experimental findings verify that, in comparison to previous designs, the suggested method lowers total latency and on-chip power. Additionally, the architecture may be scaled from 4-bit to 16-bit, making it suitable for a range of applications, including digital signal processing, embedded systems, and cryptographic systems.

RFERENCES

[1] Efficient VLSI Architecture Integrating Vedic Mathematics for Square Computation UG Patil, P Jagtap, K Adake, S Dhanbhar, A Paithane
[2] Journal of VLSI Circuits and Systems, 2025•vlsijournal.com Squaring Circuit Using 14nmFinFET Technology with Vedic Mathematics Approach S Shetkar, S Koli
[3] IETE Journal of Research, 2024•Taylor & Francis Vedic Multiplier for High-Speed Applications JVR Sudhamsu Preetham, P Nethra… - … , Software and Networks …, 2022 – Springer
[4] Analysis of Low Power Approximate 128x128 bit Vedic Multiplier for Existing Real-World FPGAs S Kamatchi, h prasad 2024 5th ieee global conference for advancement in technology (gcat), 2024•ieeexplore.ieee.org
[5] FPGA implementation of a resource efficient vedic multiplier using SPST adders KV Gowreesrinivas, S Srinivas, P Samundiswary Engineering, Technology & Applied Science Research, 2023•mail.etasr.com
[6] Design and performance analysis of low power and energy-efficient vedic multipliers S Shaik, S Kanapala, V Vijay, CS Pittala - International Journal of System …, 2023 – Springer
[7] Design a DSP Operations using Vedic Mathematics P Sreemantha, MB Jyothirmayee - academia.edu
[8] Design of efficient binary multiplier architecture using hybrid compressor with FPGA implementation V Thamizharasan, V Parthipan - Scientific Reports, 2024 - nature.com
[9] Performance analysis of 32-bit Vedic multipliers for different adder configurations R Raj, S Darsana, P Ramesh 2022 IEEE 19th India council international conference , 2022•ieeexplore.ieee.org
[10] Design of a Squaring Architecture Based on Yavadunam Sutra of Vedic Mathematics CG Yadav, GS Reddy… - … Conference on Visual …, 2025 - ieeexplore.ieee.org
[11] Efficient approximate multipliers utilizing compact and low-power compressors for error-resilient applications B Vakili, O Akbari, B Ebrahimi - AEU-International Journal of Electronics …, 2024 – Elsevier
[12] Efficient FPGA Implementation of RSA Algorithm Using Vedic Multiplier KJ Jegadish Kumar, P Kaythry, V Gokhulesh… - researchgate.net
[13] Design of efficient binary multiplier architecture using hybrid compressor with FPGA implementation V Thamizharasan, V Parthipan - Scientific Reports, 2024 - nature.com
[14] Design of a Squaring Architecture Based on Yavadunam Sutra of Vedic Mathematics CG Yadav, GS Reddy… - … Conference on Visual …, 2025 - ieeexplore.ieee.org
[15] Design and Implementation of an Optimized High-Speed Vedic-Based Squarer Circuit Using Reversible Logic Gates S Halder, ML Saha, Malvika, J Talukdar… -… Conference on Micro …, 2023 – Springer
[16] S. Senthazhai1, V. Kokila2, P. Janani3, M. Keerthana4, A. Rajeshwari5, S. Deepa6: 04 | Apr 2025 (IRJET)
[17] An improved squaring circuit for binary numbers K Sethi, R Panda International Journal of Advanced Computer Science and Applications, 2012•academia.edu
[18] Approximate arithmetic circuit architectures for FPGA-based systems S Ullah, A Kumar - 2023 – Springer
[19] A modular technique of Booth encoding and Vedic multiplier for low-area and high-speed applications CM Kalaiselvi, RS Sabeenian - Scientific Reports, 2023 - nature.com

ISSN 2250-3676 ijesatj@gmail.com https://www.ijesat.com/